SYNCHRONIZATION OF TWO OR MORE VIDEO PLAYERS

BACKGROUND OF THE INVENTION

This invention relates to a synchronizer for synchronous recovery of video signals from two or more video players, and to a video player system incorporating such a synchronizer in addition to two or more video players and one or more displays.

By the term "video player," as used herein and in the claims appended hereto, is meant a player, with or without recording facilities, of any video storage media, such as those in tape form, as in the case of a video tape recorder (VTR), and in disk form, as in the case of a videodisk player as typified by a digital versatile disk (DVD) player. The invention is applicable to any such video players as well as to a system of two or more such video players together with one or more displays.

It has been known and practiced conventionally to synchronously drive two or more VTRs, for example, for simultaneous reproduction of as many correlated video signals on separate displays or on separate sections or windows of one display screen. Japanese Unexamined Patent Publication No. 52-56513 to Matsushita Electric is hereby cited as describing and claiming how to synchronize two or more video VTRs for use with video tapes having longitudinal picture and sound tracks. Essentially, it teaches to compare the phases of the vertical synchronizing pulses, included in the recovered video signals, with that of a series of reference pulses from a source external to the tapes or to the VTRs. The drive motors for the rotary drums carrying the magnetic heads, or those for the capstans, of both VTRs are controlled so as to keep the vertical sync pulses of the video signals being reproduced, in phase with the external reference pulses.

An objection to this prior art method is that it necessitates the provision of a source of accurately timed reference pulses. Such a pulse source is costly and would make the resulting synchronizer significantly more expensive than in the absence thereof.

SUMMARY OF THE INVENTION

The present invention seeks to attain synchronous driving of two or more video players without relying on any reference signal other than the standard vertical sync pulses prerecorded on the video tapes or other storage media.

Briefly, the invention may be summarized as a synchronizer for compulsorily synchronizing a plurality of video players for simultaneous presentation of as many correlated pictures on a display or displays, each video player being for use with a video storage medium on which there is stored a video signal including a series of vertical sync pulses. The synchronizer comprises a plurality of vertical sync pulse separator circuits to be connected one to each video player for separating the series of vertical sync pulses from a video signal being recovered from the video storage medium. Connected to the pulse separator circuits is a reference moment determination circuit for determination of a reference moment in prescribed time relationship to each vertical sync pulse of one selected series of such pulses being supplied from either of the pulse separator circuits. A play synchronization circuit is connected to both of the vertical sync pulse separator circuits and the reference moment determination circuit for production of a plurality of phase departure signals each indicative of a phase departure, if any, of each vertical sync pulse of one series of such pulses from the reference moment determined in relation to one associated vertical sync pulse of the selected series of such pulses. The phase departure signals are for delivery one to each video player for causing the video players to produce the series of vertical sync pulses in phase with each other.

In order to better illustrate the principles of this invention, let us consider the simplest case of how two video players, or two series of vertical sync pulses being thereby recovered from video storage media, are synchronized according to the invention. If the first series of vertical sync pulses lag in phase behind the second series, the reference moment determination circuit will determine, in one preferred embodiment of the invention, a reference moment at the trailing edge of each pulse of the first series.

In putting the reference moment signal and the two series of ver-

tical sync pulses, the play synchronization will then a first and a second phase departure signal for the first and the second series of vertical sync pulses. The first phase departure signal will now contain no significant pulse because the reference moment has been determined to be at the trailing edge of each vertical sync pulse of the first series. The second phase departure signal will do, however, contain a pulse having a duration in proportion to the phase departure of each vertical sync pulse of the second series. This second phase departure signal is utilized, for example, to accelerate the capstan motor of the first video player into phase with the second.

It is thus seen that the invention dispenses with a dedicated source of timing pulses for phase comparison of the two or more series of vertical sync pulses. The synchronizer according to the invention is therefore manufacturable much more inexpensively than the conventional devices incorporating such reference pulse sources.

The above and other objects, features and advantages of the invention and the manner of realizing them will become more apparent, and the invention itself will best be understood, from the following description taken together with the attached drawings showing the preferred embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing the synchronizer according to the present invention as incorporated in a two-VTR, two-display system by way of one possible application of the invention;

FIG. 2 is a schematic diagram, partly in block form, showing in more detail the two VTRs of the FIG. 1 embodiment together with the synchronizer according to the invention;

FIG. 3 is a block diagram showing those functional means in the controller of one of the two VTRs of FIG. 2 which have relevance to the synchronizer according to the invention, the controller of the other VTR being of identical design;

FIG. 4 is a block diagram showing in some more detail the synchronizer of the FIG. 1 embodiment together with those parts of the VTRs which are directly associated with the synchronizer;

FIG. 5 is a schematic electrical diagram, partly in block form, of the play synchronization circuit of the FIG. 4 synchronizer;

FIG. 6 is a schematic electrical diagram of the VTR status judgment circuit included in the FIG. 5 play synchronization circuit;

FIG. 7 is a diagram of waveforms of signals appearing in various parts of the FIG. 5 play synchronization circuit during compulsory synchronization of the two FIG. 1 VTRs in the case where no phase difference exists between the two series of vertical sync pulses from the VTRs;

FIG. 8 is a waveform diagram similar to FIG. 7 but showing the same signals in the case where the first series of vertical sync pulses, from one of the two FIG. 1 VTRs, are delayed in phase from the second series of such pulses from the other VTR;

FIG. 9 is also a waveform diagram similar to FIG. 7 but showing the same signals in the case where the second series of vertical sync pulses are delayed in phase from the first series of such pulses;

FIG. 10 is a block diagram of a three-VTR, three-display video player system employing the synchronizer according to the invention;

FIG. 11 is a somewhat more detailed block diagram of the synchronizer of the FIG. 10 embodiment, shown together with some pertinent output and input terminals of the three VTRs;

FIG. 12 is a schematic electrical diagram of the play synchronization circuit of the FIG. 11 synchronizer;

FIG. 13 is a diagram of waveforms of signals appearing in various parts of the FIG. 12 play synchronization circuit during compulsory synchronization of the three FIG. 10 VTRs in the case where no phase difference exists between the three series of vertical sync pulses from the VTRs;

FIG. 14 is a waveform diagram similar to FIG. 13 but showing the same signals in the case where the three series of vertical sync pulses, from the three FIG. 10 VTRs, all differ in phase from one another;

FIG. 15 is also a waveform diagram similar to FIG. 13 but showing the same signals in the case where a phase difference exists between the first and the third series of vertical sync pulses and where the second of the three FIG. 10 VTRs is not in play mode;

FIG. 16 is a schematic electrical diagram of a slight modification of

the FIG. 5 play synchronization circuit;

FIG. 17 is a schematic electrical diagram of a slight modification of the FIG. 12 play synchronization circuit; and

FIG. 18 is a partial schematic electrical diagram of an additional slight modification of the play synchronization circuit according to the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will now be described in detail as applied by way of example to the two-VTR, two-display video player system illustrated in FIG. 1. The exemplified video player system has a first 1*a* and a second 1*b* VTR of like design, a first 2*a* and a second 2*b* display which also are of identical make, and a play synchronizer 3 forming the gist of the invention. The VTRs 1*a* and 1*b* are both conventionally equipped to record composite video signals, including picture signals as well as synchronizing and blanking pulses, on magnetic tapes in cassette form, not shown in this figure, and later reproduce and send them to the displays 2*a* and 2*b*, respectively, for visual presentation of two correlated pictures. Alternatively, the video signals from both VTRs may be directed into one display, as indicated by the broken-line arrow in this figure, for reproduction of the two pictures on separate parts or windows of the same screen.

The play synchronizer 3 is shown connected to both VTRs 1*a* and 1*b* as a synchronization adapter, so to say, for compulsorily synchronizing them during playback operation by deriving the series of standard vertical sync pulses from the composite video signals being recovered from the commercially available tape cassettes by both VTRs. Relying on these vertical sync pulses, the play synchronizer 3 produces what are herein termed phase departure signals, which are directed back into both VTRs for compulsorily synchronizing them as manifested by the phasing of the all the series of vertical sync pulses.

Reference may be had to FIG. 2 for more detailed study of the VTRs 1*a* and 1*b*. Since the two VTRs are of similar construction, like reference numerals will be used to denote like parts of both devices, as well as of the tape cassettes shown loaded therein, only with the letters

a and *b* suffixed to such numerals to denote which VTR the parts belong to. Only the first VTR 1*a* will be detailed, it being understood that the same description applies to the second 1*b*.

Essentially constructed according to the standard VHS design, the representative VTR 1*a* is for use with a commercially available video tape cassette 4*a* wherein a length of magnetic tape 7*a* has its opposite extremities anchored to a pair of reels 5*a* and 6*a* to run bidirectionally therebetween. It is understood that a video signal is recorded on the tape 7*a* along a series of slanting tracks in conformity with, for example, the NTSC or PAL standards. As is well known, the standard video signal includes the vertical sync pulses, in addition to the visual information, that are transmitted at the end of each field to keep the receiver in field-by-field synchronism with the transmitter. The picture is blanked during each vertical retrace period, when the electron beam is returned to the top of the screen at the end of one field. The tape 7*a* has also a control signal recorded longitudinally thereon.

Pulled out the cassette 4*a* and guided by guide pins, the tape 7*a* is wrapped a required angle over a rotary drum 8*a* to which a pair of magnetic read/write heads or transducers 8*a* and 9*a* are mounted in diametrically opposite positions thereon. The tape 7*a* is wound on the drum 8*a* at such an angle to its axis as to enable the transducers to trace the slanting tracks thereon. A drum motor 11*a* is drivingly coupled to the drum 8*a*. It is to be understood that the transducers 8*a* and 9*a* as well as their electrical connections are shown highly schematically in FIG. 2 by way of illustration and explanation.

Along the tape path from one reel to the other of the cassette 4*a* there are sequentially arranged a control head 12*a*, an audio head, not shown, an erase head, also not shown, and a cooperative combination of capstan 13*a* and pinch roller 14*a*. A capstan motor 15*a* is drivingly coupled to the capstan 13*a* for constant speed tape travel. Tachometers 16*a* and 17*a* are coupled to the drum motor 11*a* and capstan motor 15*a*, respectively, for feedback speed control of the motors. The drum 8*a* carries in a prescribed position on its circumference a part 18*a* to be sensed or detected by a head or detector 19*a* for switching between the transducers 8*a* and 9*a*.

Also included in the representative VTR 1*a* are a tape transport

20*a*, a signal processing network 21*a*, a controller 22*a*, a drum motor driver circuit 23*a*, and a capstan motor driver circuit 24*a*. Drivingly coupled to the cassette reels 5*a* and 6*a*, tape transport 20*a* operates under the direction of the controller 22*a* for causing bidirectional tape travel therebetween.

The signal processing network 21*a* is electrically connected to the pair of transducers 9*a* and 10*a* on the drum 8*a* for conventionally processing the video signals recovered from the tape and those to be recorded thereon. More specifically, the network 21*a* comprises a transducer switching circuit, a video amplifier, and a frequency-demodulator for processing the signals recovered, and a frequency-modulator and a recording amplifier for processing the signals to be recorded. The network 21*a* is shown connected to two video output terminals 25*a* and 26*a* for production of the video signals.

The controller 22*a* is connected to all of the control head 12*a*, tachometers 16*a* and 17*a*, transducer switching position detector 19*a*, tape transport 20*a*, signal processing network 21*a*, drum motor driver circuit 23*a*, and capstan motor driver circuit 24*a*, as well as to the play synchronizer 3 which is external to the VTR 1*a*. The controller 22*a* is per se of conventional make including a microprocessor for performing a variety of control functions.

For the purposes of this invention, however, the controller 22*a* may be considered comprising the means depicted block-diagrammatically in FIG. 3; namely, a drum motor servo circuit 31*a*, a tape transport control circuit 32*a*, a signal processing network control circuit 33*a*, a capstan motor servo circuit 34*a*, a play command circuit 35*a*, a tape-end detector circuit 36*a*, and a sync pulse separation control circuit 37*a*.

The drum motor servo circuit 31*a* has an input connected to the transducer switching position detector 19*a*, and another input to the drum motor tachometer 16*a*, both shown in FIG. 2, for producing a control signal for the drum motor 11*a* in response to the outputs therefrom. The control signal is delivered to the drum motor driver circuit 23*a*, FIG. 2.

The tape transport control circuit 32*a* controls the tape transport 20*a*, FIG. 2. The signal processing network control circuit 33*a* controls the signal processing network 21*a*, FIG. 2.

The capstan motor servo circuit 34*a* has an input connected to

the control head 12*a*, and another input to the tachometer 17*a*, both shown in FIG. 2, for producing a tape speed control signal for causing the capstan motor 15*a* to drive the tape 7*a* at a required speed. The tape speed control signal is supplied to the capstan motor driver circuit 24*a*, as well as to the play synchronizer 3 by way of a first controller output terminal 38*a*.

The play command circuit 35*a* responds to the actuation of a play switch, not shown, by the user by delivering a play command to the play synchronizer 3 from a second controller output terminal 39*a*. The play command is of course utilized internally of the VTR 1*a*, too, by means that are not shown because of impertinence to the invention.

The tape-end detector circuit 36*a* has an output connected to a third controller output terminal 40*a* for providing a signal indicative of whether the tape has been run to the predetermined end of the tape (EOT). The EOT signal is also delivered to the play synchronizer 3 from the third controller output terminal 40*a*.

The sync pulse separation control circuit 37*a* has an output connected to a fourth controller output terminal 41*a* for providing a control signal for separation of the vertical sync pulses from the recovered video signal. This control signal is also fed to the play synchronizer 3 from the fourth controller output terminal 41*a*.

In FIG. 4 is shown in more detail the play synchronizer 3 in combination with some directly associated parts of the VTRs 1*a* and 1*b*. The play synchronizer 3 is herein shown, however, only in terms of three component circuits into which it is broadly divisible, more detailed illustration being to be presented subsequently. The three constituent circuits are two vertical sync pulse separator circuits 42*a* and 42*b* for separation of the vertical sync pulses from the video signals being recovered from the tapes in the VTRs 1*a* and 1*b*, respectively, and a play synchronization circuit 43 for production of the play synchronization signals for delivery back to the VTRs.

The first vertical sync pulse separator circuit 42*a* of the play synchronizer 3 has an input connected to the signal processing network 21*a* of the first VTR 1*a* via the video output 26*a*, and another input to the sync pulse separation control circuit 37*a*, FIG. 3, of the controller 22*a* of the first VTR via the fourth controller output terminal 41*a*. The sec-

ond vertical sync pulse separator circuit 42*b* of the play synchronizer 3 has an input connected to the signal processing network 21*b* of the second VTR 1*b* via the video output 26*b*, and another input to the sync pulse separation control circuit of the controller 22*b* of the second VTR via the fourth controller output terminal 41*b*.

So connected to the necessary parts of the VTRs 1*a* and 1*b*, the vertical sync pulse separator circuits 42*a* and 42*b* derive the vertical sync pulses from the video signals supplied from the VTRs and deliver to the play synchronization circuit 43 one rectangular output pulse per field. The separation of sync pulses from video signals is familiar to television specialists, so that no more detailed illustration or description of the sync pulse separator circuits 42*a* and 42*b* is deemed necessary. These circuits 42*a* and 42*b* could be built into the VTRs 1*a* and 1*b*, respectively.

As indicated also in FIG. 4, the play synchronization circuit 43 has inputs connected to the two vertical sync pulse separator circuits 42*a* and 42*b* by way of lines 44*a* and 44*b*, to the first to third controller output terminals 38*a*, 39*b* and 40*a* of the first VTR 1*a* by way of lines 45*a*, 46*a* and 47*a*, and to the first to third controller output terminals 38*b*, 39*b* and 40*b* of the second VTR 1*b* by way of lines 45*b*, 46*b* and 47*b*. The play synchronization circuit 43 has two output lines 48*a* and 48*b* connected to the input terminals 49*a* and 49*b*, and thence to the capstan motor driver circuits 24*a* and 24*b*, of the VTRs 1*a* and 1*b*, respectively.

Inputting the two vertical sync pulse signals from the separator circuits 42*a* and 42*b*, the play synchronization circuit 43 operates to compare their phases one with respect to the other. For such phase comparison this circuit 43 determines a reference moment in prescribed time relationship to each pulse of one of the two input signals and provides phase departure signals indicative of a possible phase departure of each pulse of each input signal with respect to that reference moment. The phase departure signals are delivered one to each VTR for controlling the speeds of the capstan motors 15*a* and 15*b*. Since each pulse of said one input signal has no phase departure from the reference moment, only the capstan motor associated with the other input signal has its speed readjusted for synchronizing this other signal with said one.

The reader's attention is now invited to FIG. 5 for closer study of the play synchronization circuit 43 of the play synchronizer 3. Broadly, the play synchronization circuit 43 comprises a VTR status judgment circuit 50 for ascertaining whether both VTRs 1*a* and 1*b* are in condition for compulsory play synchronization according to the invention, a reference moment determination circuit 51 for establishment of a reference moment with respect to each vertical sync pulse of either of the two incoming series of such pulses, two NOT circuits 52 and 53, two *D* flip-flops 54 and 55 as phase comparators for providing the phase departure signals, and two adders 56 and 57.

As shown in detail in FIG. 6, the VTR status judgment circuit 50 has two NOT circuits 58 and 59, and three AND gates 60, 61 and 62, although these AND gates could be input-inverting NOR gates. The first AND gate 60 has one input connected to the play command circuit 35*a*, FIG. 3, of the controller 22*a* of the first VTR 1*a* by way of the line 46*a*, and another input to the EOT detector circuit 36*a*, FIG. 3, of the controller 22*a* via the NOT circuit 58 and by way of the line 47*a*. Likewise, the second AND gate 61 has one input connected to the equivalent of the play command circuit 35*a* in the controller 22*b* of the second VTR 1*b* by way of the line 46*b*, and another input to the equivalent of the EOT detector circuit 36*a* in the controller 22*b* via the NOT circuit 59 and by way of the line 47*b*.

The third AND gate 62 of the VTR status judgment circuit 50 has its two inputs connected to the first two AND gates 60 and 61. The output of the AND gate 62, and of the complete VTR status judgment circuit 50, is connected to the reference moment determination circuit 51, FIG. 5, by way of a line 63. It is thus seen that the judgment circuit 50 judges that the VTRs 1*a* and 1*b* are in condition for compulsory synchronization when both VTRs are in play mode and, at the same time, when the tapes 7*a* and 7*b* are both not driven to their ends. The judgment circuit 50 will go high when all these conditions prove to be met.

With reference back to FIG. 5 the reference moment determination circuit 51 of the play synchronization circuit 43 comprises a *D* flip-flop 64, a OR gate 65, a NOR gate 66, a NAND gate 67, and an AND gate 68. The OR gate 65 has its two inputs connected to the vertical sync

pulse separator circuits 42*a* and 42*b*, FIG. 4, by way of the noted input lines 44*a* and 44*b*, respectively, and its output to the clock input *T* of the flip-flop 64. This flip-flop 64 will be hereinafter referred to as the reference moment flip-flop in contradistinction from the flip-flops 54 and 55 of the play synchronization circuit 43, which will then be referred to as the play synchronization flip-flops.

The NOR gate 66 has one input connected to the *Q* output of the play synchronization flip-flop 54, another input to the *Q* output of the other play synchronization flip-flop 55, and an output to the data input *D* of the reference moment flip-flop 64. The NAND gate 67 has its two inputs likewise connected respectively to the *Q* outputs of the play synchronization flip-flops 54 and 55. The AND gate 68 has one input connected to the output line 63 of the VTR status judgment circuit 50, another input to the NAND gate 67, and an output to the reset or clear input *R* of the reference moment flip-flop 64. The preset input *PR* of this flip-flop 64 is connected to a positive supply terminal designated *+V*.

The play synchronization flip-flop 54 has a trigger input *T* connected to the first vertical sync signal input line 44*a* via the NOT circuit 52, a data input *D* and a preset input *PR* both connected to a positive supply terminal *+V*, and a reset input *R* connected to the *Q* output of the reference moment flip-flop 64.

The other play synchronization flip-flop 55 has a trigger input *T* connected to the second vertical sync signal input line 44*b* via the NOT circuit 53, a data input *D* and a preset input *PR* both connected to a positive supply terminal *+V*, and a reset input *R* connected to the *Q* output of the reference moment flip-flop 64.

Both play synchronization flip-flops 54 and 55 are to be reset when their reset inputs *R* go low. These play synchronization flip-flops are intended as aforesaid for production of phase departure pulses for eliminating a phase differences, if any, between the two series of vertical sync pulses from the VTRs 1*a* and 1*b*. Each flip-flop will put out such phase departure pulses during the vertical retrace periods, one pulse for each field.

The adder 56 has one input connected to the *Q* output of the play synchronization flip-flop 54, another input connected by way of the

line 45*b* to the equivalent of the capstan motor servo circuit 34*a*, FIG. 3, in the controller 22*b* of the second VTR 1*b*, and an output connected by way of the line 48*b* to the capstan motor driver circuit 24*b*, FIGS. 2 and 4, of the second VTR 1*b*. The capstan motor 15*b* is therefore driven according to the addition of the output from the capstan motor servo circuit in the second VTR controller 22*b* and the output from the play synchronization flip-flop 54.

The other adder 57 has one input connected to the *Q* output of the other play synchronization flip-flop 55, another input connected by way of the line 45*a* to the capstan motor servo circuit 34*a*, FIG. 3, of the controller 22*a* of the first VTR 1*a*, and an output connected by way of the line 48*a* to the capstan motor driver circuit 24*a*, FIGS. 2 and 4, of the first VTR 1*a*. The capstan motor 15*a* is likewise driven according to the addition of the output from the capstan motor servo circuit 34*a* and the output from the play synchronization flip-flop 55.

Operation

The operation of the two-VTR video player system, particularly of the play synchronizer 3, constructed as hereinbefore described with reference to FIGS. 1-6, will be best understood by referring to the waveform diagrams of FIG. 7-9. The following indicia will be used to denote some pertinent signals associated with the play synchronizer in the following operational description of the player system:

Vs_1 = first series of vertical sync pulses from the first vertical sync pulse separator circuit 42*a*

Vs_2 = second series of vertical sync pulses from the second vertical sync pulse separator circuit 42*b*

V_{65} = output from the OR gate 65 of the reference moment determination circuit 51

V_{54} = output from the play synchronization flip-flop 54, equivalent to the phase departure signal to be applied to the second VTR 1*b* or the phase difference between the first vertical sync pulses *Vs1* and the output *V64* of the flip-flop 64

V_{55} = output from the other play synchronization flip-flop 55, equivalent to the phase departure signal to be applied to the VTR 1*a* or the phase difference between the second vertical sync pulses *Vs2* and the output *V64* of the flip-flop 64

V_{64} = output from the reference moment flip flop 64

V_{66} = output from the NOR gate 66 of the reference moment determination circuit 51

V_{67} = output from the NAND gate 67 of the reference moment determination circuit 51

V_{68} = output from the AND gate 68 of the reference moment determination circuit 51.

FIG. 7 represents the foregoing voltage signals appearing in the various parts of the play synchronization circuit 43, FIG. 5, when no phase difference exists between the two series of vertical sync pulses Vs_1 and Vs_2 derived from the video signals from the VTRs 1*a* and 1*b* by the sync pulse separator circuits 42*a* and 42*b*; FIG. 8 the same voltage signals when the sync pulses Vs_1 from the first VTR lag in phase behind the sync pulses Vs_2 from the second VTR; and FIG. 9 the same voltage signals when the sync pulses from the first VTR have a phase advance over those from the second VTR.

The VTR status judgment circuit 50, FIG. 6, of the play synchronization circuit 43 will go high as aforesaid when both VTRs 1*a* and 1*b* are in play mode and, at the same time, when the tapes 7*a* and 7*b* are not run to their ends. The reference moment flip-flop 64, FIG. 5, will then be not reset but operate to permit forced synchronization of the two VTRs.

On the other hand, when either or both of the VTRs 1*a* and 1*b* are not in play mode, or when the tape end is reached in either or both of these VTRs, the VTR status judgment circuit 50 will go low to indicate that the VTRs are not fit for synchronization. The AND gate 68, FIG. 5, of the reference moment determination circuit 51 will then also go low, resetting the flip-flop 64 and so making its Q output go low, too. This low output being applied to the reset inputs R of both play synchronization flip-flops 54 and 55, the play synchronization circuit 43 will not operate.

Incidentally, in the FIG. 5 play synchronization circuit 43, the NAND gate 67 will go low when both flip-flops 54 and 55 go high. The AND gate 68 will then also go low, resetting the reference moment flip-flop 64. The play synchronization flip-flops 54 and 55 will be thereby reset in turn.

Let us now assume that the VTRs 1*a* and 1*b* are now in condition for compulsory synchronization according to the invention. Supplied from the vertical sync pulse separator circuits 42*a* and 42*b*, FIG. 4, over their output lines 44*a* and 44*b*, the sync pulses Vs_1 and Vs_2 will be inverted in polarity by the NOT circuits 52 and 53 before being applied to the clock inputs of the play synchronization flip-flops 54 and 55, respectively. These flip-flops 54 and 55 will take in the high input to their data input terminals *D* at the moments of the trailing edges of the incoming vertical sync pulses, that is, of the rises of the outputs from the NOT circuits 52 and 53. However, being under the control of the reference moment flip-flop 64, the play synchronization flip-flops 54 and 55 will not remain set for any significant period of time, as will become better understood as the description proceeds.

If then the series of vertical sync pulses Vs_1 and Vs_2 from both VTRs 1*a* and 1*b* are in phase with each other as has been assumed above in conjunction with FIG. 7, the output pulses V_{65} of the OR gate 65, FIG. 5, will also be in phase with these vertical sync pulses. Clocked by the leading edges of these OR gate output pulses V_{65}, the reference moment flip-flop 64 will take in the output V_{66} from the NOR gate 66 through its data input *D*. The NOR gate output V_{66} is shown in FIG. 7 to be high (H) at t_1 when the outputs V_{54} and V_{55} from the play synchronization flip-flops 54 and 55 are both low (0). Consequently, the output V_{64} from the reference moment flip-flop 64 will go high at t_1 at the moment of the leading edge of the output pulse V_{65} of the OR gate 65. Thus the play synchronization flip-flops 54 and 55 will both become operable at t_1.

Then, clocked at t_2 by the trailing edges of the vertical sync pulses Vs_1 and Vs_2, or by the rises of the outputs from the NOT circuits 52 and 53, the play synchronization flip-flops 54 and 55 will take in their data inputs *D*. The play synchronization flip-flop outputs V_{54} and V_{55} will thus go high at t_2. The output V_{67} from the NAND gate 67 of the reference moment determination circuit 51 will go low in response to these high inputs from the play synchronization flip-flops 54 and 55, thereby causing the reference moment flip-flop 64 to be reset by the output V_{68} from the AND gate 68.

The moment the reference moment flip-flop 64 is thus reset is the

reference moment needed for play synchronization of the VTRs 1*a* and 1*b* according to the instant invention. As the reference moment flip-flop 64 is reset as above, so will be the play synchronization flip-flops 54 and 55. Therefore, as indicated in FIG. 7, the play synchronization flip-flop outputs V_{54} and V_{55} will go high only momentarily at t_2. It will also be noted from FIG. 7 that the NAND gate output V_{67}, AND gate output V_{68} and NOR gate output V_{66} will all go low momentarily at t_2. When the series of vertical sync pulses Vs_1 and Vs_2 from both VTRs 1*a* and 1*b* are in phase with each other as in FIG. 7, the play synchronization flip-flop output pulses V_{54} and V_{55} will be so short in duration that they are not to affect the traveling speed of the cassette tapes 7*a* and 7*b* even though they are applied via the adders 56 and 57 to the capstan motor driver circuits 24*a* and 24*b*, FIG. 4. Aside from these play synchronization pulses of negligibly short durations, the driver circuits 24*a* and 24*b* will input the capstan motor servo signals by way of the lines 45*a* and 45*b*, for causing the capstan motors 15*a* and 15*b* to be driven accordingly.

Both vertical synch pulses Vs_1 and Vs_2 recur, of course, with a cycle Tv in FIG. 7. What has happened from t_1 to t_2, as explained above, will repeat itself from t_3 to t_4 and so forth.

Let us now proceed to FIG. 8 for discussion of what occurs when the vertical sync pulses Vs_1 from the first VTR 1*a* slightly lag in phase from those Vs_2 from the second 1*b*, "slightly" because there is no time spacing between every two associated sync pulses from both VTRs. The play synchronization circuit 43 will then operate to bring the first VTR 1*a* into phase with the second 1*b* through the procedure set forth hereinbelow.

It will be observed from FIG. 8 that, in this case, each of the OR gate output pulses V_{65} has a duration, as from t_1 to t_3, equal to the sum of the duration, as from t_2 to t_3, of one vertical sync pulse Vs_1 from one VTR and the duration, as from t_1 to t_2, of one associated vertical sync pulse Vs_2 from the other VTR. Clocked by the leading edge of each such OR gate output pulse V_{65}, the reference moment flip-flop 64 will go high at t_1, enabling the play synchronization flip-flops 54 and 55.

So enabled, the play synchronization flip-flop 55 will first go high

at t_2 when the NOT circuit 53 goes high in response to the trailing edge of one vertical sync pulse Vs_2 from the second VTR. Then the other play synchronization flip-flop 54 will go high at t_3 when the NOT circuit 52 goes high in response to the trailing edge of the vertical sync pulse Vs_1 from the first VTR 1*a* that immediately follows the pulse Vs_2. Both play synchronization flip-flops 54 and 55 being thus high at t_3, the NAND gate 67 will go low instantly, resetting the reference moment flip-flop 64 via the AND gate 68.

The moment t_3 the reference moment flip-flop 64 is reset as above is the reference moment in the case of FIG. 8, when both play synchronization flip-flops 54 and 55 will also be reset. Their outputs V_{54} and V_{55} are therefore shown to go low at t_3. The play synchronization flip-flop 54 has now completed the production of a pulse of negligibly short duration, whereas the other play synchronization flip-flop 55 has produced a pulse of much longer duration, lasting from t_2 to t_3.

One cycle of operation of the play synchronization circuit 43, in response to one vertical sync pulse Vs_1 from the first VTR and one associated similar pulse Vs_2 from the second VTR, has now been completed. The next similar cycle will occur as the two associated vertical sync pulses are input from t_4 to t_6 in FIG. 8.

Each FIG. 8 output pulse V_{54} of the play synchronization flip-flop 54 is too brief to take significant part in speed control of the magnetic tape 7*b*, FIG. 2, in the second VTR 1*b*, just as the output pulses V_{54} and V_{55} of both play synchronization flip-flop 54 and 55 were when both series of vertical sync pulses Vs_1 and Vs_2 were in synchronism with each other as in FIG. 7. It is the magnetic tape 7*a* in the first VTR 1*a* that needs speed readjustment for synchronous driving with the tape 7*b*.

To that end, each output pulse V_{55} of the other play synchronization flip-flop output 55 has its duration determined in proportion with the phase difference between the two series of vertical sync pulses Vs_1 and Vs_2, to take active part in tape speed control in the first VTR 1*a*. The adder 57, FIG. 5, of the play synchronization circuit 43 will add each such play synchronization flip-flop output pulse and the capstan motor servo signal fed from the capstan motor servo circuit 34*a*, FIG. 3, of the first VTR controller 22*a* over the line 45*a*. The resulting output from the adder 57 will be delivered to the capstan motor driver circuit 24*a*,

FIG. 4, of the first VTR 1*a* over the line 48*a*.

The capstan motor driver circuit 24*a* comprises an input selector switch 69*a* and an amplifier 70*a*. The input selector switch 69*a* is shown to have one fixed contact connected to the controller 22*a*, another fixed contact connected to the VTR output 49*a* and thence to the play synchronization circuit 43 by way of the line 48*a*, and a movable contact for selectively connecting the two fixed contacts to the amplifier 70*a*. FIG. 4 also shows the capstan motor driver circuit 24*b* of the second VTR 1*b*, which is of like construction.

The input selector switch 69*a* is to choose the play synchronization circuit 43 when the video player system is in play synchronization mode, and the VTR controller 22*a* when it is not. The addition of the capstan motor servo signal and the play synchronization signal is therefore amplified and applied to the capstan motor 15*a* in play synchronization mode, and only the capstan motor servo signal amplified and applied to the capstan motor in non-play-synchronization mode. The same holds true with the second VTR capstan motor driver circuit 24*b*.

Referring once again to FIG. 8, the play synchronization flip-flop output pulse V_{55} that is produced right after each vertical sync pulse Vs_2 will be combined with the capstan motor servo signal from the first VTR controller 22*a* for joint delivery to the capstan motor driver circuit 24*a*. The first VTR capstan motor 15*a* will be accelerated during the t_2-t_3 duration of the play synchronization flip-flop output pulse V_{55} for bringing the first tape 7*a* into phase with the second tape 7*b*.

Possibly, the delay of the first tape 7*a* may not be overcome by the single output pulse V_{55} of the play synchronization flip flop 55. Then a required number of such pulse will be produced, as from t_5 to t_6 in FIG. 8, for reaccelerating the first VTR capstan motor 15*a* until synchronism is attained between both series of vertical sync pulses from the VTRs 1*a* and 1*b* as in FIG. 7. Normally, the vertical sync pulses are recovered at a rate of one for each one sixtieth of a second, with errors of no more than several percent. If there is an error of 2.5 percent, for instance, then the time per field is as short as 0.000425 second. Synchronism is therefore attainable with minimal speed readjustment of one of the capstan motors 15*a* and 15*b* relative to the other.

It is also to be appreciated in connection with FIG. 8 that the

t_2-t_3 or t_5-t_6 duration of each play synchronization flip-flop output pulse V_{55} is so determined as to coincide, and not to exceed, each vertical retrace period of the video signal. The capstan motor 15*a* is therefore readjusted in speed without affecting the picture being exhibited on the screen.

In FIG. 9 are shown the vertical sync pulses Vs_2 from the second VTR 1*b* lagging in phase from those Vs_1 from the first 1*a*, with a time spacing between every two associated sync pulses from both VTRs. The second VTR 1*b* is to be accelerated into phase with the first 1*b* in this case, as will be detailed hereinbelow.

Inputting the two series of vertical sync pulses Vs_1 and Vs_2, the OR gate 65, FIG. 5, of the reference moment determination circuit 51 will produce the output V_{65} composed of both series of vertical sync pulses. First clocked at t_1 by the leading edge of one of the first series of vertical sync pulses Vs_1, the reference moment flip-flop 64 will go high by taking in the NOR gate output V_{66}, enabling both play synchronization flip-flops 54 and 55. Clocked at t_2 by the trailing edge of the first vertical sync pulse Vs_1, the first play synchronization flip-flop 54 will take in its data input and so go high at that moment. This high output V_{54} will cause the NOR gate 66 to go low at t_2.

Upon appearance of the associated one of the second series of vertical sync pulses Vs_2 at t_3, the OR gate 65 will again go high, clocking the reference moment flip-flop 64. Its data input D being then low, the reference moment flip-flop 64 will go low at t_3, thereby resetting both play synchronization flip-flops 54 and 55. One output pulse from the play synchronization flip-flop 54 has now been terminated. The other play synchronization flip-flop 55 will not respond to the trailing edge of the vertical sync pulse Vs_2 appearing at t_3, staying low.

The play synchronization flip-flop output V_{54} will be added by the adder 56 to the capstan motor servo signal fed from the second VTR controller 22*b* over the line 45*b*. The resulting adder output will be delivered over the line 48*b* to the second VTR capstan motor driver circuit 24*b*, FIG. 4, in which the adder output will be directed by the input selector switch 24*b* into the amplifier 70*b* preparatory to delivery to the second VTR capstan motor 15*b*. This motor will then be accelerated instantaneously to bring the lagging second VTR video tape 7*b* into

phase with the first VTR video tape 7*a*. If the second series of vertical sync pulses Vs_2 does not come into synchronism with the first s_1 by the single play synchronization pulse V_{54}, the foregoing cycle of operation from t_1 to t_3 will be repeated, as from t_4 to t_5, until synchronization is achieved.

The advantages gained by this first preferred embodiment of the invention may be recapitulated as follows:

1. The two VTRs 1*a* and 1*b* can be compulsorily synchronized for playback of the correlated recordings on the two video tapes 7*a* and 7*b* by the external play synchronizer 3 of simple construction composed of only the sync pulse separator circuits 42*a* and 42*b* and the play synchronization circuit 43.

2. No dedicated reference signal is used; instead, a reference moment signal is produced from the vertical sync pulses from both VTRs in order to produce in turn a play synchronization signal for accelerating the capstan motor of the lagging VTR according to the phase difference between the two series of vertical sync pulses. The circuitry of the resulting play synchronizer is simpler and less expensive in configuration than the prior art employing a dedicated reference signal source.

3. Capstan motor speed readjustment in response to a pulse or pulses from either of the play synchronization flip-flops 54 and 55 is made during vertical retrace, so that the pictures being displayed are not affected in any way by the compulsory synchronization.

4. The play synchronization signals according to the invention are combined with the standard capstan motor servo signals prior to delivery to VTRs, in which selection is made by the input selector switches 24*a* and 24*b* between the capstan motor servo signals alone and the combination of the play synchronization signals and capstan motor servo signals. So constructed, the play synchronizer 3 lends itself to use as an external adapter of commercially available VTRs.

5. Connected in circuit with the VTRs 1*a* and 1*b*, the play synchronization circuit 43 will nevertheless operate only when the VTRs are in condition for forced play synchronization, thanks to the provision of the VTR status judgment circuit 50.

Second Form

The invention is herein applied to the three-VTR, three-display video player system shown in FIG. 10. The three VTRs 1*a*, 1*b* and 1*c* are of identical design, the third VTR 1*c* being similar to the VTRs 1*a* and 1*b* shown in FIG. 2, and so are the three displays 2*a*, 2*b* and 2*c*. The pertinent parts of the third VTR 1*c* will be identified by suffixing the letter *c* to the reference numerals used to denote the corresponding parts of the VTRs 1*a* and 1*b*. As in the first disclosed embodiment, the VTRs 1*a*-1*c* may be either independently coupled to the respective displays 2*a*-2*c*, as indicated by the solid lines in this figure, or to one display, as indicated by the dashed lines. At 3′ is shown a play synchronizer according to the instant invention which is adapted for use with the three VTRs 1*a*-1*c*.

As depicted block-diagrammatically in FIG. 11, the modified play synchronizer 3′ is broadly divisible into a first 42*a*, a second 42*b* and a third 42*c* vertical sync pulse separator circuit for deriving the vertical sync pulses from the composite video signals recovered from the tapes by the three VTRs 1*a*, 1*b* and 1*c*, respectively, and a play synchronization circuit 43′ for creating play synchronization signals from the derived vertical sync pulses. The three vertical sync pulse separator circuits 42*a*-42*c* are of like configuration, the third circuit 42*c* being similar to the first two circuits 42*a* and 42*b*. Suffice it to say, therefore, that the third vertical sync pulse separator circuit 42*c* is connected to the video output terminal 26*c* and fourth controller output terminal 41*c* of the third VTR 1*c* for separating the vertical sync pulses Vs_3 from the third video output, and to the play synchronization circuit 3′ for delivery of the vertical sync pulses thereto.

The play synchronization circuit 43′ is designed on the same principles as the FIG. 5 play synchronization circuit 43 for production of capstan motor control signals, composed of play synchronization signals according to the invention and conventional capstan motor servo signals, which are applied to the three VTRs 1*a*-1*c* for their play synchronization. Toward this end the play synchronization circuit 43′ is connected to the vertical sync pulse separator circuits 42*a*-42*c* by way of lines 44*a*-44*c* to the output terminals 38*a*, 39*a*, 49*a* and input terminal 49*a* of the first

VTR 1*a*, to the output terminals 38*b*, 39*b* and 40*b* and input terminal 49*b* of the second VTR 1*b*, and to the output terminals 38*c*, 39*c* and 40*c* and input terminal 49*c* of the third VTR 1*c*. The terminals 26*c*, 38*c*-40*c* and 49*c* of the third VTR 1*c* correspond to the terminals 26*a*, 38*a*-40*a* and 49*a* of the first VTR 1*a*. Although the connection of the second output line 48*b* of the play synchronization circuit 3 is not clearly indicated in FIG. 11 for illustrative convenience, it is understood that the output line 48*b* is connected to the terminal 49*b* of the second VTR 1*b*, just as the output line 48*b* of the play synchronization circuit 43, FIG. 4, is shown connected to the terminal 49*b* of the second VTR.

As illustrated in more detail in FIG. 12, the play synchronization circuit 3′ comprises a third *D* flip-flop 70 for play synchronization in addition to the two noted play synchronization flip-flops 54 and 55 of the first embodiment, a third adder 88 in addition to the two noted adders 56 and 67, three AND gates 71, 72 and 73, a reference moment determination circuit 51′ which is an adaptation of the FIG. 5 reference moment determination circuit 51 for use with three VTRs, three NOT circuits 81, 82 and 83, a three-input OR gate 84, and three AND gates 85, 86 and 87.

Instead of the VTR status judgment circuit 50, FIG. 5, of the first disclosed play synchronization circuit 43, the modified synchronization circuit 43′ has the three AND gates 71-73 having their inputs connected respectively to the vertical sync pulse separator circuits 42*a*-42*c* by way of the vertical sync pulse lines 44*a*-44*c* on the one hand and, on the other, to the play command output terminals 39*a*-39*c*, FIG. 3, of the VTRs 1*a*-1*c* by way the lines 46*a*-46*c*. Thus are the vertical sync pulses Vs_1-Vs_3 allowed through the AND gates 71-73 only when high inputs indicative of play commands are being input from the controllers of the VTRs 1*a*-1*c*. Any undesired operation of the play synchronization circuit 43′, triggered for instance by noise, is thus precluded when the VTRs 1*a*-1*c* are in other than play mode.

The three play synchronization flip-flops 54, 55 and 70 have their clock inputs *T* connected to the AND gates 71-73, respectively, their data inputs *D* and preset inputs *PR* connected to a positive supply terminal +*V*, and their reset inputs *R* to the reference moment determination circuit 51′.

The reference moment determination circuit 51′ has three OR gates 74, 75 and 76 connected respectively to the *Q* outputs of the play synchronization flip-flops 54, 55 and 70 on the one hand and, on the other, to the play command lines 46*a*-46*c* via NOT circuits 78, 79 and 80. An NAND gate 77, another component of the reference moment determination circuit 51′, have inputs connected to the three OR gates 74-76, and an output connected as aforesaid to the reset inputs *R* of the play synchronization flip-flops 54, 55 and 70. Alternatively, the OR gates 74-76 could be coupled directly to the flip-flops 54, 55 and 70.

The OR gate 84 has its three inputs connected respectively to the *Q* outputs of the play synchronization flip-flops 54, 55 and 70. The output of this OR gate 84 is connected to all of the three-input AND gates 85-87, the other inputs of which are connected respectively to the *Q* outputs of the play synchronization flip-flops 54, 55 and 70 via the NOT circuits 81-83, and to the play command lines 46*a*-46*c*. The AND gates 85-87 could be connected directly to the inverting outputs of the play synchronization flip-flops 54, 55 and 70.

The first adder 56 has one input connected to the capstan motor servo line 45*a* of the first VTR 1*a*, another input to the AND gate 85, and an output to the line 48*a* leading to the input terminal 49*a* of the capstan motor driver circuit 24*a*, FIG. 4, of the first VTR. The second adder 57 has one input connected to the capstan motor servo line 45*b* of the second VTR 1*b*, another input to the AND gate 86, and an output to the line 48*b* leading to the input terminal 49*b* of the capstan motor driver circuit 24*b* of the second VTR. The third adder 88 has one input connected to the capstan motor servo line 45*c* of the third VTR 1*c*, another input to the AND gate 87, and an output to the line 48*c* leading to the input terminal 49*c* of the capstan motor driver circuit of the third VTR. Thus the adders 56-58 provide additions of the standard capstan motor servo signals from the VTRs controllers and the play synchronization signals from the AND gates 85-87, for delivery to the capstan motor driver circuits of the VTRs 1*a*-1*c*.

Operation of Second Form

Reference may be had to the waveform diagrams of FIGS. 13-15

for the following discussion of the operation of the three-VTR video player system of FIGS. 10-12. The following indicia will be used to denote the pertinent signals appearing in various parts of the FIG. 12 play synchronization circuit 43′ in the following operational description:

V_{71} = Vs_1 = first series vertical sync pulses from the first vertical sync pulse separator circuit 42*a*

V_{72} = Vs_2 = second series of vertical sync pulses from the second vertical sync pulse separator circuit 42*b*

V_{73} = Vs_3 = third series of vertical sync pulses from the third vertical sync pulse separator 42*c*

V_{54} = output from the first play synchronization flip-flop 54

V_{55} = output from the second play synchronization flip-flop 55

V_{70} = output from the third play synchronization flip flop 70

V_{74} = output from the first OR gate 74 of the reference moment determination circuit 51′

V_{75} = output from the second OR gate 75 of the reference moment determination circuit 51′

V_{76} = output from the third OR gate 76 of the reference moment determination circuit 51′

V_{77} = output from the NAND gate 77 of the reference moment determination circuit 51′

V_{84} = output from the OR gate 84

V_{85} = output from the AND gate 85

V_{86} = output from the AND gate 86

V_{87} = output from the AND gate 87.

FIG. 13 represents the foregoing voltage signals when the three series of vertical sync pulses Vs_1, Vs_2 and Vs_3 from the three VTRs 1*a*, 1*b* and 1*c* are all in synchronism with one another; FIG. 14 the same voltage signals when the sync pulses Vs_1 from the first VTR 1*a* are advanced in phase over those from the other VTRs 1*b* and 1*c*; and FIG. 15 the same voltage signals when the sync pulses Vs_3 from the third VTR 1*c* has a phase advance over those Vs_1 from the first 1*a*, with the second VTR 1*b* being in stop mode.

The three play synchronization flip-flops 54, 55 and 70, FIG. 12, of the play synchronization circuit 43′ will all be clocked by the three series of vertical sync pulses Vs_1-Vs_3 if all the VTRs 1*a*-1*c* are in play

mode. Let us assume that all these series of vertical sync pulses are in phase as in FIG. 13. The Q outputs V_{54}, V_{55} and V_{70} from the flip-flops 54, 55 and 70 will all go high as at t_1 in FIG. 13 in response to the leading edges of each vertical sync pulse of each series. These high outputs from cause the three OR gates 74-76 of the reference moment determination circuit 51' go high, too, thereby making the NAND gate 77 go low. The low output V_{77} will reset all the three flip-flops 54, 55 and 70 instantly after they have gone high at t_1 as above. As the flip-flop outputs V_{54}, V_{55} and V_{70} become low again after the instantaneous high state at t_1, the output V_{77} from the reference moment determination circuit 51' will become high again immediately after that moment, enabling the flip-flops 54, 55 and 70.

The OR gate 84 will also respond to the instantaneous pulses from all the flip-flops 54, 55 and 70, itself instantaneously going high at t_1, as indicated at V_{84} in FIG. 13. Although this instantaneous output pulse of the OR gate 84 is applied to the three AND gates 85-87, these AND gates will also input the inversions, by the NOT circuits 81-83, of the flip-flop output pulses V_{54}, V_{55} and V_{70} at t_1, so that the AND gate outputs V_{85}-V_{87} will remain low.

No play synchronization pulses will thus be input to the adders 56-58. Directed from the three VTR controllers over the lines 45*a*-45*c*, the capstan motor servo signals only will be fed over the play synchronization circuit output lines 48*a*-48*c* to the capstan motor driver circuits of the three VTRs. No phase readjustment will occur in the VTRs in response to the vertical sync pulses input to the phase synchronization circuit 43' from t_1 to t_2.

The play synchronization circuit 43' will repeat the foregoing cycle of operation in response to each set of three vertical sync pulses incoming at the cycle Tv. No phase readjustment will occur, either, as long as each such set of pulses remain in phase as in FIG. 13.

In FIG. 14 are shown the first series of vertical sync pulses Vs_1 as having a phase advance over the other two series Vs_2 and Vs_3; the second series of vertical sync pulses Vs_2 as having a phase lag from the other two Vs_1 and Vs_3; and the third series of vertical sync pulses Vs_3 as having a phase lag from the first Vs_1 and a phase advance over the second Vs_2. The first pulse of the first series of vertical sync pulses

Vs_1 is shown to appear from t_1 to t_2, the first pulse of the second series Vs_2 from t_4 to t_5, and the first pulse of the third series Vs_3 from t_2 to t_3.

In that case, out of the three flip-flops 54, 55 and 70, the first flip-flop 54 will first go high at t_1 in response to the leading edge of one of the first series of vertical sync pulse Vs_1. Then the third flip-flop 70 will go high at t_2 in response to the leading edge of one of the third series of vertical sync pulses Vs_3. Finally, the second flip-flop 55 will go high at t_4 in response to the leading edge of one of the second series of vertical sync pulses Vs_2.

At t_4, therefore, the three flip-flops 54, 55 and 70 will all be high, making the NAND gate 77 of the reference moment determination circuit 51' go low. All the flip-flops 54, 55 and 70 will in turn be reset by this low output from the circuit 51', themselves going low after t_4. Then the NAND gate 77 will go high again after having been momentarily low at t_4 and so enable the flip-flops 54, 55 and 70 for the vertical sync pulses to be supplied subsequently.

A closer observation of FIG. 14 will reveal that the pulse thus produced by the first flip-flop 54 rises at t_1 with the rise of one first vertical sync pulse Vs_1 and decays at t_4 with the rise of one second vertical sync pulse Vs_2. The output pulse of the second flip-flop 55 rises and decays almost concurrently at t_4. The output pulse of the third flip-flop 70 rises at t_2 with the rise of one third vertical sync pulse Vs_3 and decays also at t_4.

In short the pulses issuing from the flip-flops 54, 55 and 70 during the t_1-t_4 period have durations equal to the time differences between the leading edge, at t_4 (reference moment in this case), of one second vertical sync pulses Vs_2, which is the most delayed, and the leading edges, at t_1, t_4 and t_2, respectively, of the three associated vertical sync pulses Vs_1-Vs_3. Thus, as in the previous embodiment of the invention, the reference moment determination circuit 51' functions to provide a series of reference moments, and the flip-flops 54, 55 and 70 to ascertain the phase departures of the three series of vertical sync pulses with respect to the reference moments.

Inputting the three flip-flop outputs V_{54}, V_{55} and V_{70}, the OR gate 84 will be high from t_1 to t_4 in FIG. 14. The inversions, by the

NOT circuits 81-83, of the flip-flop outputs V_{54}, V_{55} and V_{70} will be allowed through the AND gates 85-87 only during the t_1-t_4 period. The resulting output from the first AND gate 85 will be low during this period, so that no speed change of the capstan motor will be made for synchronization purposes in the first VTR 1*a*, which is now assumed to be most advanced in the phase of the vertical sync pulses. The capstan motor of the first VTR 1*a* will, instead, be controlled solely by the capstan motor servo signal fed from the first VTR controller.

Since the inversion of the second flip-flop output V_{55} during the t_1-t_4 period is high except at t_4, the resulting output from the second AND gate 86 will be high throughout the period. Added to the capstan motor servo signal from the second VTR controller at the second adder 57, the high output from the second AND gate 86 will cause a corresponding acceleration of the capstan motor of the second VTR 1*b*, which is now assumed to be most delayed, in order to bring the second series of vertical sync pulses Vs_2 into phase with the first Vs_1.

The inversion of the third flip-flop output V_{70} is high from t_1 to t_2 and low from t_2 to t_4, the resulting output from the third AND gate 87 will be high from t_1 to t_2. This third AND gate output V_{87} will be added to the capstan motor servo signal from the third VTR controller at the third adder 88 for delivery to the third VTR capstan motor driver circuit. The third VTR capstan motor will be accelerated from t_1 to t_2 for bringing the third series of vertical sync pulses Vs_3 into phase with the first Vs_1.

The three VTRs 1*a*-1*c* may, or may not, be synchronized solely by the foregoing cycle of operation taking place from t_1 to t_4 in FIG. 14. The same cycle will be repeated as required after t_6 until synchronization is achieved.

FIG. 15 has been drawn on the assumption that only the first and third VTRs 1*a* and 1*c* are in play mode and that the first series of vertical sync pulses VS_1 lag in phase behind the third series of vertical sync pulses Vs_3. In this case the play synchronizer 3' is required to accelerate the first VTR 1*a* into synchronism with the third 1*c*.

The third flip-flop 70 will go high upon appearance of one third vertical sync pulse Vs_3 at t_1, causing the third OR gate 76 of the reference moment determination circuit 51' to go high at that moment. The

first flip-flop 54 will go high upon appearance of one first vertical sync pulse Vs_1 at t_3, likewise causing the first OR gate 74 of the reference moment determination circuit 51' to go high at that moment. Since the second VTR 1*b* is now not in play mode, the second play command line 46*b* will be low, so that the NOT circuit 79 and therefore the second OR gate 75 will both be high.

At t_3, therefore, all the inputs to the NAND gate 77 of the reference moment determination circuit 51' will become high, causing the NAND gate to go low. All the flip-flops 54, 55 and 70 will thus be reset t_3. The first and third flip-flops 54 and 70 will then go low, whereas the second flip-flop 55 has been low. The OR gate 84 will therefore be high from t_1 to t_3, and so will be the AND gate 85. The high output V_{85} from the AND gate 85 will be added by the adder 56 to the first VTR capstan motor servo signal, and the resulting adder output delivered to the first VTR capstan motor driver circuit for accelerating the first VTR capstan motor. Here again the same cycle of operation will be repeated after t_5 in FIG. 15 until the first 1*a* and the third 1*c* VTRs become synchronized.

If, contrary to the showing of FIG. 15, the second VTR 1*b* were in play mode, too, the second series of vertical sync pulses Vs_2 would be allowed through the AND gate 72. Depending upon the phase relations of the second series of vertical sync pulses Vs_2 to the other two series of such pulses Vs_1 and Vs_3, they will undergo a different procedure for synchronization therewith. Details of such a synchronization procedure are considered self-evident from the foregoing description of FIGS. 13-15.

It is now clear that the present invention is equally well applicable to both two- and three-VTR display systems. In the case of the three-VTR system of FIGS. 10-12, too, a reference moment is set up in relation to the most delayed one of each set of three associated vertical sync pulses. The phase relations of each set of vertical sync pulses relative to the reference moment are determined by the flip-flops 54, 55 and 70, and capstan motor acceleration pulses are produced accordingly. The three series of vertical sync pulses are forced into exact synchronization by use of simple and inexpensive electronics comprising the flip-flops and logic circuits.

The advantages gained by this three-VTR system are akin to those set forth in connection with the two-VTR system. Additionally, any two of the three VTRs, in addition to all three, may be played synchronously.

Third Form

FIG. 16 shows a slight modification 43*b* of the two-VTR play synchronization circuit 43, FIG. 5. The modified play synchronization circuit 43*b* features subtracters 56′ and 57′ employed in lieu of the adders 56 and 56 of the circuit 43. The subtracters 56′ and 57′ have positive inputs connected to the first and the second VTR capstan motor servo lines 45*a* and 45*b*, negative inputs connected to the *Q* outputs of the flip-flops 54 and 55, and outputs connected by way of the lines 48*a* and 48*b* to the first and the second VTR capstan motor driver circuits 24*a* and 24*b*, FIG. 4, respectively. The modified play synchronization circuit 43*b* is analogous with the FIG. 5 circuit 43 in the other details of construction.

In operation, if the two series of vertical sync pulses Vs_1 and Vs_2 have the phase relationship depicted in FIG. 8, for instance, then the output V_{55} from the second flip-flop 55 will be subtracted from the second VTR capstan motor servo signal. The result will be the deceleration of the second VTR capstan motor, until the second series of vertical sync pulses Vs_2 are delayed into phase with the first Vs_1.

Fourth Form

The three-VTR play synchronization circuit 43′ of FIG. 12 is likewise modifiable as in FIG. 17. The modified play synchronization circuit 43*c* incorporates three subtracters 56′, 57′ and 88′ in places of the adders 56, 57 and 88 of the FIG. 12 circuit 43′. The subtracters 56′, 57′ and 88′ have positive inputs connected to the VTR capstan motor servo lines 45*a*, 45*b* and 45*c*, negative inputs connected to the *Q* outputs of the flip-flops 54, 55 and 70 via two-input AND gates 85′, 86′ and 87′ only, and outputs connected by way of the lines 48*a*, 48*b* and 48*c* to the three capstan motor driver circuits, respectively. The AND gates 85′-87′

have their other inputs connected to the play command lines 46*a*-46*c*, respectively. The other details of construction are as previously set forth with reference to FIG. 12.

If the three series of vertical sync pulses Vs_1-Vs_3 have the phase relationship of FIG. 14, for instance, the outputs V_{64} and V_{70} from the flip-flops 54 and 70 will be subtracted from the first and the third VTR capstan motor servo signals on the lines 45*a* and 45*c*. The first and the third VTR capstan motors will then be decelerated until the first and the third series of vertical sync pulses Vs_1 and Vs_3 are delayed into phase with the second Vs_2 which have been most delayed.

Fifth Form

The adders 56 and 57 of FIG. 5 and adders 56, 57 and 88 of FIG. 12 may all be each replaced by a signal selector circuit shown in FIG. 18 and therein generally designated 90. The representative signal selector circuit 90 is a simple combination of an on-off switch 91 and a reverse-blocking diode 92. The switch 91 is connected between the capstan motor servo line 45*a*, 45*b* or 45*c* and the play synchronization circuit output line 48*a*, 48*b* or 48*c*. Preferably a transistor or like electronic switch, the switch 91 is normally closed, opening in response to a pulse on the play synchronization signal line 93, which in fact is the output line of the flip-flop 54 or 55 in FIG. 5 or of the AND gate 85, 86 and 87 in FIG. 12. The play synchronization signal line 93 is connected to the play synchronization circuit output line 48*a*, 48*b* or 48*c* via the diode 92.

The capstan motor servo signal will travel freely through the signal selector circuit 90 when the play synchronization circuit 43 or 43′ is producing no pulses, for constant speed servo control of the associated capstan motor. The switch 91 will open in response to, say, the t_2-t_3 pulse V_{55}, FIG. 8, from the flip-flop 55, FIG. 5, so that only this pulse will be allowed through the signal selector circuit 90 for accelerating the second VTR capstan motor. In use of this signal selector circuit 90 the voltage amplitude of the play synchronization pulses on the line 93 may be made higher than the maximum voltage of the capstan motor servo signal on the line 45*a*, 45*b* or 45*c*.

The subtracters 56′ and 57′ of FIG. 16 and subtracters 56′, 57′ and 88′ of FIG. 17 may also be each replaced by this signal selector circuit 90, provided that play synchronization pulses for deceleration control of the capstan motors are input over the line 93.

Possible Modifications

Despite the foregoing detailed disclosure it is not desired that the present invention be limited by the exact showings of the drawings or by the description thereof. The following is a brief list of possible modifications, alterations and adaptations which are all intended in the illustrated embodiments and so believed to fall within the scope of the invention:

1. The play synchronizer 3 could be integrated with the two VTRs 1*a* and 1*b* in the FIG. 1 video player system.

2. The play synchronizer 3′ could also be integrated with the three VTRs 1*a*-1*c* in the FIG. 10 video player system.

3. The play synchronizer 3 could be built into each of the two VTRs 1*a* and 1*b* in the FIG. 1 system, and the play synchronizer of either VTR used for play synchronization of both VTRs.

4. The play synchronizer 3′ could also be built into each of the three VTRs 1*a*-1*c* in the FIG. 10 system, and the play synchronizer of either VTR used for play synchronization of the VTRs.

5. The adders 56 and 57 of the FIG. 5 play synchronization circuit 43, the adders 56, 57 and 88 of the FIG. 12 circuit 43′, the subtracters 56′and 57′ of the FIG. 16 circuit 43*b*, and the subtracters 56′, 57′ and 88′ of the FIG. 17 circuit 43*c* could be built into the capstan motor driver circuits of the VTRs 1*a*-1*c*, with the switches, such as those shown at 69*a* and 69*b* in FIG. 4, omitted.

6. In the FIGS. 5 and 16 play synchronization circuit 43 and 43′, the outputs from the flip-flops 54 and 55 could be directed into the adders 56 and 57, or subtracters 56′ and 57′, via integrating circuits or lowpass filters.

7. In the FIGS. 12 and 17 play synchronization circuits 43′ and 43*c*, too, the outputs from the AND gates 85-87 or 85′-87′ could be directed into the adders 56-58, or subtracters 56′-58′, via integrating circuits or

lowpass filters.

8. In the FIGS. 10-15 embodiment, as in the FIGS. 1-9 embodiment, the vertical sync pulses Vs_1-Vs_3 could be allowed through the AND gates 71, 72 and 73 only when the tape ends are not detected during operation in play mode.

9. The invention could be applied to play synchronization of four or more VTRs.

10. The invention could be applied to synchronization of various videodisk players, in which application the speed of the videodisk drive motor, or the readout speed of the buffer memory on the input side of the digital-to-analog converter of the videodisk playback circuit, may be controlled by the outputs from, for instance, the flip-flops 54, 55 and 70.